AMENDMENTS TO SPECIFICATION

Rewrite the paragraph beginning on page 12, line 1, as follows:

Finally, as shown in Fig. 1(e), to the fourth constitution, a protection film 9 comprising silicon nitride (SiN) of about 500 nm thickness is formed by using a gas mixture such as SiH_4, NH_3 and N_2 to [[a]] an exposed surface portion by using a plasma chemical vapor deposition (CVD) apparatus. The thus formed silicon nitride (SiN) film is etched by a dry etching method using an etching gas such as SF_6 to remove an unnecessary portion and a portion of the drain electrode 7 and the source electrode 8 is exposed to complete a channel etching type thin film transistor.

Rewrite the paragraph beginning on page 20, line 16, as follows:

In a conventional method of manufacturing a channel etching type thin film transistor, since it is necessary to continuously conduct the steps for removing the photoresist in the channel portion, etching for the chromium (Cr) film and the channel etching, the controllability of the amount in each etching step is not satisfactory and stable transistor characteristics can not be obtained unless the thickness of the high resistant amorphous silicon film 4 is 200 nm or more. But, in the method of manufacturing the thin film transistor according to this invention, since the channel etching step is eliminated, [[a]] stable transistor characteristics can be obtained even when the thickness for the high resistance amorphous silicon film 4 is reduced to 50 nm and, further, when each of the steps is conducted continuously while keeping the vacuum state, the rate of occurrence for the defects of the thin film transistor caused by deposition of obstacles suspended in atmospheric air can be minimized.

Rewrite the paragraph beginning on page 27, line 4, as follows:

Hence, the present invention provides a method of fabricating a thin film transistor ~~is provided~~ comprising the steps of providing a gate over a substrate, providing a gate insulating layer over the gate and the substrate, providing a silicon layer having a first resistance over the gate insulating layer and providing an impurity over the amorphous silicon layer. The invention further provides the steps of providing a photoresist over the impurity provided silicon layer and back exposing the photoresist utilizing the gate as a mask and developing a pattern substantially identical with that of the gate and removing the pattern and forming a drain electrode and a source electrode separated by a channel region over a contact portion with the amorphous silicon. The invention further provides removing the impurity from the channel region and diffusing the impurity into the contact portion to form a contact layer wherein the contact layer has a second resistance at least lower than the first resistance.